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Control of Current Hysteresis of Networked Single-Walled Carbon Nanotube Transistors by a Ferroelectric Polymer Gate Insulator

*Yeon Sik Choi, Jinwoo Sung, Seok Ju Kang, Sung Hwan Cho, Ihn Hwang, Sun Kak Hwang, June Huh, Ho-Cheol Kim, Siegfried Bauer, and Cheolmin Park**

Films made of 2D networks of single-walled carbon nanotubes (SWNTs) are one of the most promising active-channel materials for field-effect transistors (FETs) and have a variety of flexible electronic applications, ranging from biological and chemical sensors to high-speed switching devices. Challenges, however, still remain due to the current hysteresis of SWNT-containing FETs, which has hindered further development. A new and robust method to control the current hysteresis of a SWNT-network FET is presented, which involves the non-volatile polarization of a ferroelectric poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) gate insulator. A top-gate FET with a solution-processed SWNT-network exhibits significant suppression of the hysteresis when the gate-voltage sweep is greater than the coercive field of the ferroelectric polymer layer (≈50 MV m^{-1}). These near-hysteresis-free characteristics are believed to be due to the characteristic hysteresis of the P(VDF-TrFE), resulting from its non-volatile polarization, which makes effective compensation for the current hysteresis of the SWNT-network FETs. The onset voltage for hysteresis-minimized operation is able to be tuned simply by controlling the thickness of the ferroelectric film, which opens the possibility of operating hysteresis-free devices with gate voltages down to a few volts.

1. Introduction

A two-dimensional (2D) network of single-walled carbon nanotubes (SWNTs) is one of the most promising active channel materials for field-effect transistors (FETs). It has been extensively studied for a variety of electronic device applications ranging from biological and chemical sensors to high-speed switching devices.[1–5] One of the most challenging issues hindering the further utilization of networked SWNT transistors is the large hysteresis in the transfer characteristics of the source-drain current as a function of gate voltage. The hysteresis has three distinct causes. One is preferential charge doping into the SWNTs by atmospheric moieties such as water and oxygen molecules surrounding the surface of the nanotubes.[6–9] Another is field-induced charges trapped and located at the gate insulator/air interface close to the nanotubes, for example, silanol groups on a Si oxide surface.[10] The third origin of hysteresis is extra mobile charges associated with an insulating oxide layer, including fixed oxide charges, oxide trap charges, and mobile oxide charges.[11–14] Complex interactions between these factors frequently result in current hysteresis, which increases with a gate-voltage sweep.

A variety of strategies have been proposed to control hysteresis; these strategies are aimed at minimizing the amount of external charges directly in contact with the SWNT surface. The passivation of SWNT channels and the silicon oxide insulator with humidity-inert materials[7] and self-assembled monolayers[15–17] has been shown to reduce current hysteresis efficiently. In addition, suspended carbon nanotube channels have also been found to be very effective in preventing direct contact between external charges on the substrate and the SWNT surface.[18] Other methods include the employment of graphene electrodes with few interface trap charges,[13] the control of the gate sweep rate,[12] the short-pulsed gate bias, and thermal annealing.[19] Reflecting how an increase in the gate-voltage sweep leads to more-prominent hysteresis, operation of a SWNT transistor under a low voltage can reduce hysteresis if combined with high-k dielectrics[20,21] or an ionic-electrolyte gate insulator.[22,23]

Despite significant technological success in controlling hysteresis, there are still several issues that need to be addressed. One is the fact that most of the previous studies investigated single-tube transistors, in which an individual SWNT as a channel required an elaborate device-fabrication process, which

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makes these transistors impractical for application in low-cost, solution-processible applications. In contrast, when networked SWNT channels are employed, based on sorting semiconducting tubes out of the mixture of metallic and semiconducting tubes[2,4,23] and utilizing Schottky barriers between the individual metallic and semiconducting tubes in the network,[24] it is rarely possible to completely eliminate hysteresis because of the complicated characteristics of the nanotube networks; namely, the abundance of tube-tube contacts, bundles, and multiple tube-electrode contacts. In other words, the perfect protection of a complex SWNT-network from external charges by direct contact elimination is almost impossible in networked SWNT FETs.[13,17] A method that can control current hysteresis and effectively suppress the hysteresis of an FET containing networked SWNT channels directly exposed to external charges (i.e., a contaminated network channel) is therefore in great demand.

Herein, we present a new and robust route to control the current hysteresis of SWNT-network FETs by using a ferroelectric poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) polymer gate insulator. Our method is based on compensating the current hysteresis arising from networked SWNTs with the characteristic hysteresis of P(VDF-TrFE)[25–29] resulting from its non-volatile ferroelectric polarization as schematically illustrated in **Figure 1**a. We demonstrate that current hysteresis in a top-gate FET with a solution-processed SWNT network is significantly suppressed when the gate-voltage sweep is greater than the coercive field of the ferroelectric polymer layer (≈50 MV m^{-1}). The control of ferroelectric film thickness thus enables a facile tuning of the onset voltage at which a near-hysteresis-free operation began. Systematic investigation suggests that onset voltage can be scaled down to low voltages. Furthermore, our networked transistor was hardly influenced by external humidity, temperature and types of substrates, allowing a wide processing window and an easy fabrication protocol.

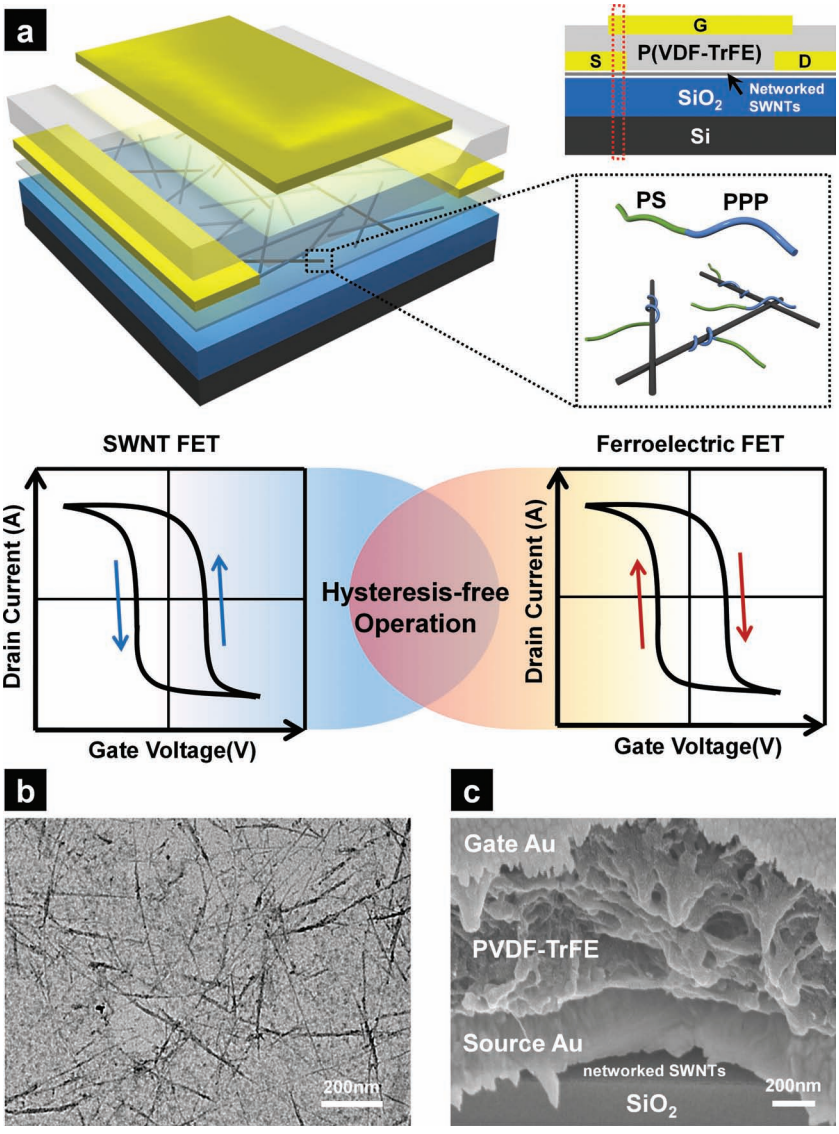

Figure 1. a) Schematics of dual-gate networked SWNT FETs. The top- and bottom-gate FETs with an SWNT-network channel contain a ferroelectric P(VDF-TrFE) layer and a dielectric SiO_2 insulator layer, respectively. The networked SWNT channel consists of individual nanotubes dispersed and covered with PS-*b*-PPP (5k/1k). A proposed hysteresis-free operation by a ferroelectric insulating layer employed in a p-type SWNT FET is shown with schematic transfer characteristics of a p-type SWNT FET and a ferroelectric FET containing a p-type semiconducting channel. b) A bright-field TEM image of a networked SWNT composite film spin-coated on the SiO_2 surface and annealed from a decanted solution of 0.02 mg mL^{-1} SWNT solution after centrifugation at 11 500 rpm. c) An SEM micrograph showing a cross-sectional view of the dual-gate FET, which corresponds to the box with red dotted lines indicated in (a).

2. Result and Discussion

To elucidate the effect of a ferroelectric polymer layer on the current hysteresis of the networked SWNT, we fabricated top and bottom dual-gate FETs sharing a solution-processed SWNT network as the active layer (Figure 1a). A thin networked SWNT film was spin-coated on a 200 nm-thick SiO_2 gate dielectric from a solution of poly(styrene-*block*-paraphenylene) (PS-*b*-PPP) (5k/1k) and SWNTs in tetrahydrofuran (THF), followed by thermal annealing at 190°C for 24 h as described in detail in our previous study.[24] The network film is flat and smooth and contains individually networked SWNTs, as well as nanotube bundles characterized by dark threads with a thickness of approximately 15 nm on average in the transmission electron microscopy (TEM) image in Figure 1b. A thin P(VDF-TrFE) film was spin-coated on the networked SWNT/block-copolymer active-channel film after the deposition of source and drain electrodes. The film was subsequently annealed at 135 °C for 2 h to increase the degree

of crystallinity. Thermal evaporation of the top Au gate electrode completed the fabrication of our dual bottom and top gate FETs with a dielectric SiO_2 layer and a ferroelectric P(VDF-TrFE) gate insulator, respectively. A cross-sectional scanning electron microscopy (SEM) image of the dual-gate FET is shown in Figure 1c, which clearly displays the semicrystalline P(VDF-TrFE) film, sandwiched between the top and source Au electrodes on the networked SWNT channel layer.

We first examined the device performance of the bottom gate FET. The I_{DS}–V_G transfer characteristics of the device showed current-modulation characteristics typical of p-type networked SWNT active layers at a forward voltage sweep from positive to negative voltages, as shown in **Figure 2**a. The devices exhibited the field-effect mobility of the metal oxide semiconductor field-effect transistor (MOSFET) standard model in the linear regime of approximately 0.5 $cm^2\ V^{-1}\ s^{-1}$ with an on/off current ratio of approximately 10^4 on average from 54 devices. When the device was swept forward from 30 V to −30 V and backward to 30 V, typical current hysteresis was observed with a hysteresis voltage window, defined as the voltage difference at an I_{DS} of approximately 10^{-10} A, of approximately 40 V. As noted, the window increased continuously with a counterclockwise hysteresis direction from a forward to a backward sweep (Figure 2a). The hysteresis observed in our system is also due to the result of complex interactions between the various causes mentioned earlier, as illustrated in Figure 2b. It should be noted that the hysteresis was not affected by the P(VDF-TrFE) layer covering the networked SWNTs, unlike a poly(methyl methacrylate) passivation layer that effectively protected the SWNT channel from environmental charged moieties.[7]

To gain insight into the origin of the hysteresis observed in the networked SWNT channel, we investigated the retention of high and low I_{DS} at zero gate voltage with time, as shown in Figure 2c. This enabled us to determine whether the current bistability arising from the SWNTs was volatile or not. Although there have been many attempts to use the characteristic current hysteresis of a SWNT-based FET as a tool of non-volatile information memory,[30,31] most of these devices exhibited poor current retention, which implies that bistable current levels from the SWNTs are transient, or volatile. Our transistor showed a similar volatile retention behavior; the low-level I_{DS} at zero gate voltage increased continuously and approached the high-level I_{DS} with time. These results suggest that our device basically works along the upward arrow as indicated in Figure 2a due to the fact that our networked SWNTs are preferentially surrounded by negatively charged species.

The ferroelectric polarization of an approximately 700 nm-thick P(VDF-TrFE) film was confirmed in a metal/ferroelectric/metal (MFM) capacitor independently fabricated with conventional polarization versus applied-voltage (P–V) hysteresis loops with different voltage sweeps, as shown in **Figure 3**a. An MFM capacitor with a P(VDF-TrFE) film treated with the same thermal-annealing conditions as we used for the dual-gate transistor showed a typical saturated hysteresis loop with a remnant polarization (P_r) and a coercive field (E_c) of approximately 8.56 μC cm^{-2} and 50.2 MV m^{-1}, respectively. The P_r of approximately 5 μC cm^{-2} at a sweep voltage of ±50 V gradually increased and remained unchanged at sweep voltages above ±70 V, as shown in Figure 3a,b.

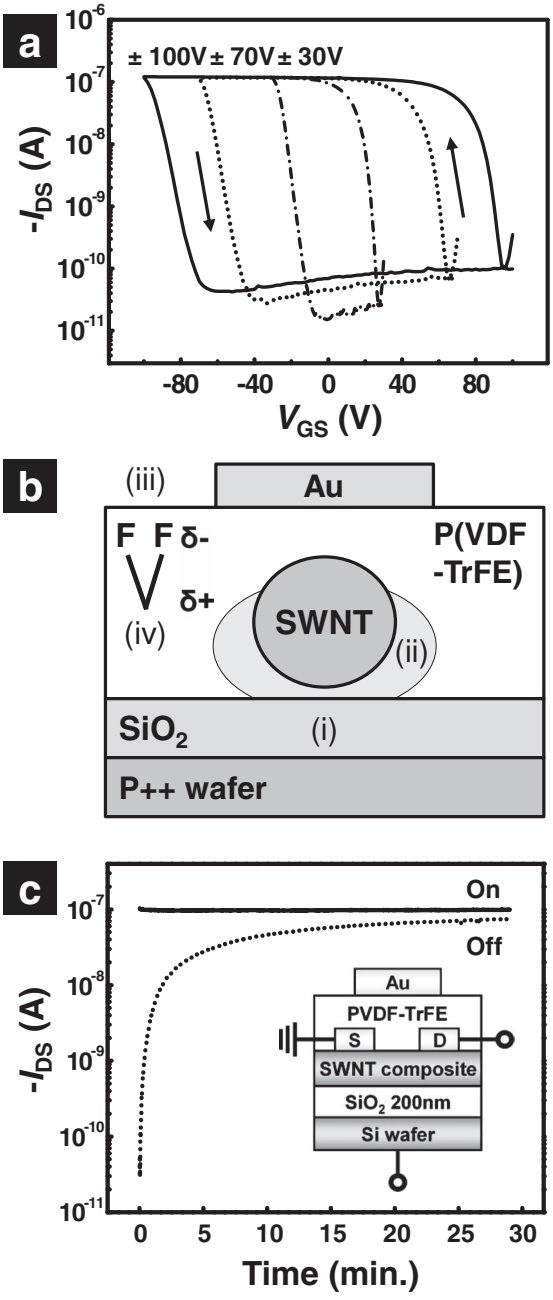

Figure 2. a) I_D–V_G transfer curves of networked SWNT FETs with SiO_2 dielectrics. The arrows indicate the direction of the development ofthe current hysteresis upon a gate-voltage sweep from a positive to a negative voltage. b) Schematic of an individual SWNT in contact with both ferroelectric P(VDF-TrFE) and the SiO_2 insulator. (i–iv) correspond to the possible origins of the current hysteresis: i) Encouragement from the insulating layer; ii) effect of charges located in the insulator/air interface close to the CNTs; iii) influence of the atmosphere environment, and iv) influence of the permanent dipole of the ferroelectric polymer dielectric. c) Retention characteristics at both high and low current levels as a function of time in a bottom-gate networked SWNT FET with a SiO_2 dielectric.

The transfer characteristics of the top-gate FET with a ferroelectric P(VDF-TrFE) gate insulator are shown as a function of the gate sweep voltage in **Figure 4**a,b. Although the transistor

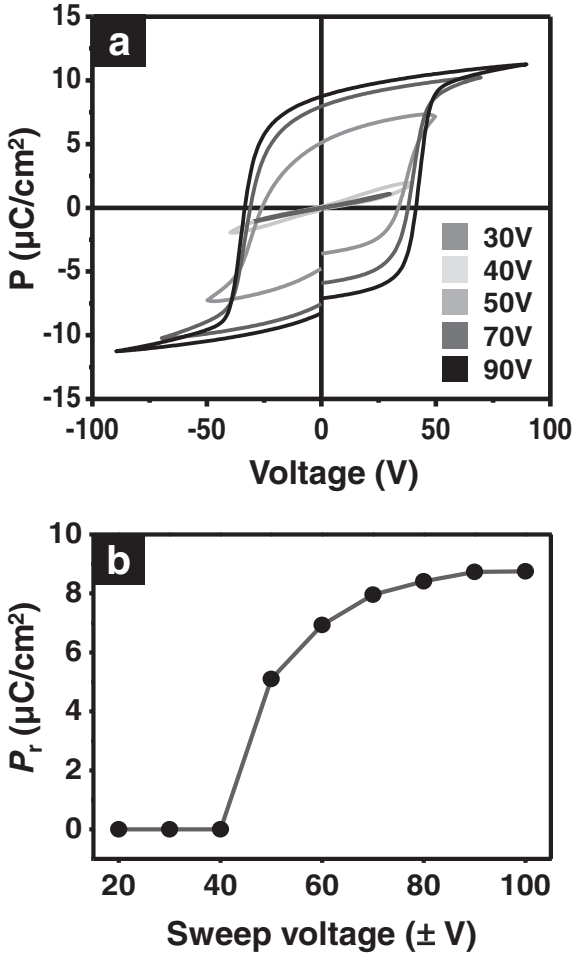

Figure 3. a) Polarization (*P*) versus applied-voltage (*V*) hysteresis loops of metal/700 nm-thick P(VDF-TrFE)/metal capacitors as a function of the sweep voltage. b) The values of remnant polarization (P_r) measured from the *P-V* hysteresis loops of metal/P(VDF-TrFE)/metal capacitors as a function of the sweep voltage. P_r increased with sweep voltage and saturated above certain sweep-voltage values.

exhibited typical p-type modulation of I_{DS} similar to that observed for the bottom-gate FET with a SiO_2 gate dielectric, the current hysteresis behavior of the networked SWNTs was very different. When the gate-voltage sweep was below approximately ±50 V, current hysteresis developed in a counterclockwise direction, and this was still observed when the voltage window increased with the voltage sweep, as shown in Figure 4a. The current hysteresis began to decrease at gate-voltage sweeps above ±50 V and near-hysteresis-free operation of the networked SWNT FET was realized at a voltage sweep of ±70 V, as shown in Figure 4b. The P(VDF-TrFE) film below its coercive field behaved as a dielectric layer, giving rise to current hysteresis because high H–F dipoles in the P(VDF-TrFE) surface provided vulnerable trap sites for charges and oxygen molecules like the SiO_2 layer. At gate-voltage sweeps above the coercive field of P(VDF-TrFE), non-volatile ferroelectric polarization developed in the film, significantly affecting the current hysteresis of the networked SWNT transistor. It should be noted, however, that the on/off ratio of a networked SWNT FET with the P(VDF-TrFE) insulator was approximately 10^2 lower than that with the SiO_2 dielectric, mainly due to a large gate leakage current through the semicrystalline P(VDF-TrFE) layer.[32]

In FETs containing ferroelectric P(VDF-TrFE) insulator as the gate dielectric layer, the polarization state of the ferroelectric layer set by the polarity of the gate voltage controls the electrical conductance of the semiconducting channel and thus distinguishes two high and low channel-current states, giving rise to current hysteresis.[29,32] In particular, a ferroelectric FET with a p-type channel exhibits typical clockwise current hysteresis, which begins with a sharp increase in I_{DS} at a negative-bias gate voltage during a forward sweep due to accumulation of excess holes in the p-type semiconductor. When the gate voltage returns to zero, the I_{DS} remains at the value saturated with the negative gate voltage because of the non-volatility of the H–F dipoles in the P(VDF-TrFE) film. The positive gate voltage subsequently applied on the device gradually switches the H–F dipoles, leading to a rapid decrease in I_{DS}. The non-volatility of the polarization should cause the current to remain the same, even after the -removal of the positive voltage. The hysteresis that develops due to the ferroelectric P(VDF-TrFE) film forms in the opposite direction to the hysteresis of an SWNT-network FET. The current hysteresis of a p-type networked SWNT FET can therefore potentially be modulated with a ferroelectric P(VDF-TrFE) insulator when the gate-voltage sweep is higher than the coercive field of the P(VDF-TrFE).

The results in Figure 4b support our hypothesis that the voltage window of the hysteresis of a networked SWNT FET should decrease with gate-voltage sweeps above ±50 V, which is greater than the coercive voltage of the P(VDF-TrFE) film in an MFM capacitor (≈35 V). The gate current between the source and gate electrodes (I_{GS}) across the P(VDF-TrFE) gate insulator measured simultaneously with I_{DS} further confirmed our hypothesis. The characteristic $\pm I_{GS}$ peaks arising from H–F dipole switching were observed at approximately ±35 V, corresponding to the coercive voltage of the P(VDF-TrFE) film with a high gate-voltage sweep above ±50 V, as shown in Figure 4d. In contrast, no specific I_{GS} variation was detected with gate-voltage sweeps of ±30 and ±40 V due to the dielectric nature of the P(VDF-TrFE) film below its coercive voltage (Figure 4c). Interestingly, current hysteresis attributed to ferroelectric switching has recently been utilized as non-volatile memory in FETs with a single SWNT channel carefully prepared either on an epitaxially grown ferroelectric insulator[33] or on a nanoscale ferroelectric dot.[34] We believe that the single-tube channels in both cases were free from the characteristic current hysteresis of the SWNTs due to minimal contamination from parasitic external charges.

We performed a more-detailed analysis of the transfer curves as a function of the gate-voltage sweep in Figures 4a and 4b by separately examining gate voltages for the turn-on and turn-off at which I_{DS} increased abruptly and then decreased from a forward to backward sweep, respectively. As shown in **Figure 5**a, the absolute value of both the turn-on and turn-off voltage increased when the gate-voltage sweep increased from ±30 to ±40 V, consistent with the results obtained for the SiO_2 dielectric layer (see Figure 2b). At a gate-voltage sweep above ±50 V, the ferroelectric switching of the P(VDF-TrFE) gate insulator

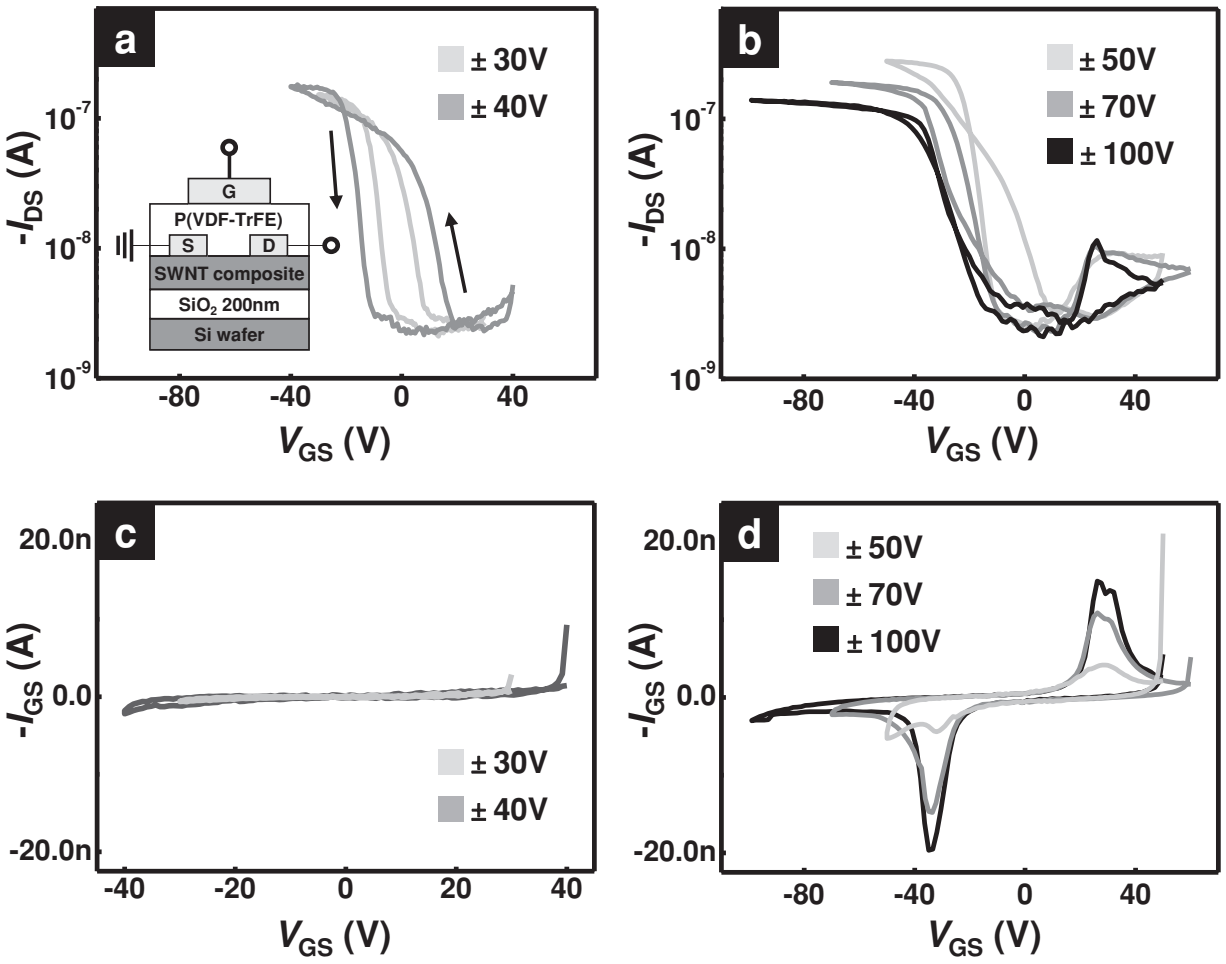

Figure 4. a,b) I_{DS}–V_G transfer curves of top-gate networked SWNT FETs with a 700 nm-thick P(VDF-TrFE) insulator as a function of the gate-voltage sweep values that was lower than (a) and higher than (b) the coercive voltage of the P(VDF-TrFE) insulator. The arrow in (a) indicates the direction of the development of the current hysteresis upon gate-voltage sweeps from a positive to a negative voltage. c,d) I_{GS}–V_G transfer curves of the top-gate networked SWNT FETs as a function of gate-voltage sweeps below (c) and above (d) the coercive voltage of the P(VDF-TrFE) film.

caused the turn-on voltage to decrease rapidly with a very gradual decrease in the turn-off voltage.

Non-volatile H–F dipoles with electron-donating H atoms pointing to the surface were formed at a positive gate voltage above the coercive voltage. When the gate voltage swept toward zero, those non-volatile ferroelectric dipoles were preserved and effectively compensated for the preferential negative charges that had accumulated around the SWNTs, making the turn-on gate voltage lower than that of the SiO_2 dielectric insulator. The charge compensation, therefore, became greater with remnant polarization of the P(VDF-TrFE) film, which in turn was proportional to the gate sweep voltage up to a certain value, as shown in Figure 4a. Consequently, the turn-on voltage decreased continuously with the sweep voltage from positive to zero and remained unchanged above ±70 V, rendering threshold voltage of a hysteresis-free transfer curve significantly shifted toward negative gate voltage as shown in Figure 4b and 5a.

The retention measurement of I_{DS} at zero gate voltage after both positive and negative gate pulses above the coercive voltage of the ferroelectric layer showed that the current level in Figure 5b (also see Supporting information, Figure S1) did not change with time over 10 000 seconds at a V_{DS} of −5 V, clearly different from the results with a bottom-gate FET with an oxide layer in Figure 2c, which implies that the shifted threshold voltage arising from our ferroelectric gate insulator is not transient. The trapped charges around the surface of SWNTs in the channel on the SiO_2 insulator were transient and the number of charges were also varied, dependent upon the gate voltage applied, clearly shown in Figure 2. The near hysteresis-free operation we observed resulted from the interplay of the transient trapped charges on the nanotube surface and the thermodynamically stable ferroelectric polarization built in the insulator rather than simple cancellation of two independent hysteresis curves. As shown in Figure 2a, the negative charges trapped to the nanotubes on SiO_2 surface at positive gate bias were dissipated when a negative gate bias was applied and no further trapping of the charges occurred till sufficient positive gate bias was applied. On the ferroelectric insulator, the trapped charges on the nanotube surface were, however, not transient

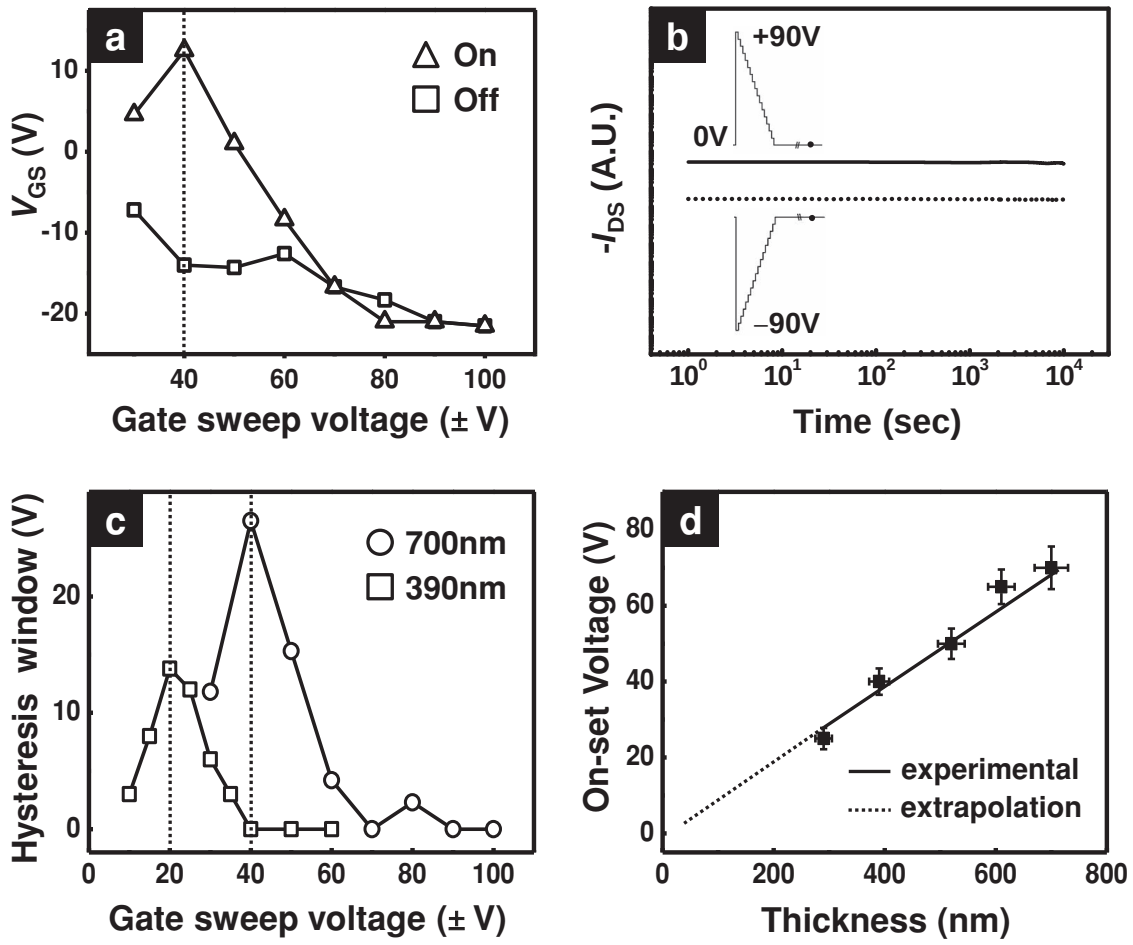

Figure 5. a) Turn-on (triangles) and turn-off (squares) gate voltages of current hysteresis that developed in top-gate networked SWNT FETs with a ferroelectric P(VDF-TrFE) insulator upon the voltage-sweep direction from positive to negative voltages. b) Retention characteristics at the two current states measured with two independent pulsed gate-voltage programs (0 → +90 → 0 and 0 → –90 → 0) as a function of time in a top-gate networked SWNT FET with a ferroelectric P(VDF-TrFE) insulator. Both currents rarely changed with time. For clear visualization, the current with the positive gate-voltage program was shifted arbitrarily. The inset shows the test sequence applied in the direct-current (DC) sweep mode for retention measurements. c) Voltage differences between the turn-on and turn-off voltages of the hysteresis curves as a function of gate-voltage sweeps in the top-gate networked SWNT FETs with ferroelectric P(VDF-TrFE) insulators of 700 nm (circles) and 390 nm (squares) in thickness. d) A plot of onset voltage for near-hysteresis-free operation of top-gate networked SWNT FETs with ferroelectric insulators as a function of the thickness of the P(VDF-TrFE) films. The dotted line corresponds to an extrapolation of the onset voltage with film thickness.

any more but pseudostable, because both trapping and dissipation of the external charges abruptly occurred in accordance with the non-volatile polarization switching of the ferroelectric layer at a certain electric field. In other words, the two remnant polarization states of the P(VDF-TrFE) layer at 0 gate voltage determined not only the mode of the hole carriers in the SWNT channel but also that of the trapped charges. This combined action gave rise to near-hysteresis-free operation. Since the trapped charges on the nanotube surface were also influenced by the remanent electric field built by the ferroelectric polarization at 0 gate voltage, the near hysteresis-free behavior was independent of the experimental-observation timescale as shown in Figure 5b.

While most of the previous studies effectively suppressed the hysteresis by passivation of SWNTs away from various causing sources, our approach, based on effective compensation of two different hysteresis curves, made top-gate networked SWNT FETs with ferroelectric insulators that were environmentally robust for controlling hysteresis. The hysteresis of the FET was suppressed with a P(VDF-TrFE) insulator at gate-voltage sweeps greater than the coercive field after lengthy exposure of the device to either oxygen gas or water vapor, which are sensitive to current hysteresis (Supporting information, Figure S2).

The combination of the turn-on and turn-off voltage behaviors resulted in the gradual reduction of the hysteresis voltage window after the maximum window at the gate-voltage sweep of near coercive voltage of a ferroelectric P(VDF-TrFE) layer, as shown in **Table 1**, and allowed for near-hysteresis-free operation of the networked SWNT FETs when a gate-voltage sweep greater than ±70 V was used. We defined this gate-voltage sweep as the onset voltage: the minimum gate sweep voltage at which near-hysteresis-free operation started to appear (Figure 5c). It should

Table 1. Characteristics of networked SWNT FETs with ferroelectric insulators, as well as MFM capacitors, as a function of the thickness of the P(VDF-TrFE) films.

Thickness [nm]	Remnant polarization[a] [μC cm^{-2}]	Coercive voltage[b] [V]	Voltage at maximum hysteresis window[b] [V]	Onset voltage for near-hysteresis-free opration[b] [V]	Saturation voltage[a] [V]
290	8.73	15	18	25	30
390	8.53	19	20	40	40
520	8.56	26	25	50	55
610	8.62	30	30	65	65
700	8.56	35	40	70	70

[a]Measured from *P*–*V* hysteresis loops; [b]Measured from I_{GS}–V_{GS} transfer curves.

be also noted from Table 1 that the onset voltage was very close to the saturation voltage of the P(VDF-TrFE) layer at which P_r was saturated in the *P*–*V* behavior.

Another important issue that should be also noted is that the near-hysteresis-free behavior was preserved even at a gate-voltage sweep greater than the saturation voltage at which the polarization of a ferroelectric polymer layer was maximized. As evidenced in Figure 2a, the surface charge density of the dielectric SiO_2 layer increased almost linearly with the gate sweep voltage until its breakdown voltage, and, in turn, the amount of the trapped and dissipated charges on the nanotube surface also increased with gate voltage, giving rise to a continuous increase of the hysteresis window with gate voltage. Different from networked SWNTs on a SiO_2 layer, the surface charge density of the ferroelectric layer did not change after its saturation, and, in consequence, the amount of trapped and dissipated external charges on the nanotube surface was saturated with the gate-voltage sweep, which indicates that the hysteresis-free operation obtained with a saturated ferroelectric polarization should be maintained even at a gate-voltage sweep greater than that for the saturation. In our 700 nm-thick P(VDF-TrFE) film, as shown in Figure 3 and 4, for instance, the gate-voltage sweep of ±70 V was enough to saturate the surface polarization, leading to near-hysteresis-free operation, which was also observed with a gate voltage of ±100 V.

To confirm further the effective control of the networked SWNT FETs with a ferroelectric P(VDF-TrFE) insulator, we employed a 390 nm-thick P(VDF-TrFE) film with a coercive voltage of approximately 20 V. We observed a continuous reduction of the hysteresis window at gate-voltage sweeps greater than 20 V, as shown in Figure 4b (also see Supporting information, Figure S3). In this case, the onset voltage was approximately ±40 V, as shown in Table 1. We also observed a controlled hysteresis operation of the networked SWNT FETs containing P(VDF-TrFE) films of different thicknesses: 610, 520, and 290 nm (Supporting information, Figure S4). A plot of the onset voltages of all of the FETs examined as a function of P(VDF-TrFE) film thickness reveals a clear linear relationship, as shown in Figure 5d and also summarized in Table 1. Considering that the coercive voltage of a ferroelectric film is linearly proportional to its thickness,[26] our results again confirm the control of the current hysteresis of SWNTs by ferroelectricity. Our results therefore suggest that networked SWNT FETs can be operated without current hysteresis over a broad range of gate-voltage sweeps from approximately 35 V to over 100 V by controlling the thickness of the ferroelectric film. Extrapolation of the plot indicates that a networked SWNT FET with an onset voltage of a few volts is possible (Figure 5d).

In our top-gate FET architecture, a P(VDF-TrFE) film less than 200 nm thick displayed significant gate leakage, making it difficult to observe p-type modulation from the SWNT-network. Low-voltage operation of the device still remains unresolved mainly due to the many structural defects and large surface roughness of P(VDF-TrFE) insulator arising from semicrystalline grain-grain mismatch, pinholes, and residual solvent trapped in the film.[29] A thick ferroelectric gate insulator is often required to minimize the electric leakage, as we have shown in our device, resulting in a high operating gate voltage greater than 50 V. Besides an approach by selecting a proper solvent that gave rise to a thin P(VDF-TrFE) film with dense chain packing,[35] most of the previous studies suggest insertion of various interlayers between the gate electrode and the ferroelectric layer including inorganic oxides and polymers. For low-voltage operation of a device, one should design a chemically, as well as electrically, robust interlayer as thin as possible with high capacitance.[36,37] Alternatively, an interlayer with a topographically patterned nanostructure has been an effective route for low-voltage operation of a FET with a P(VDF-TrFE) insulator. Nanoconfinement of ferroelectric crystals into the nanopattern significantly reduced the leakage current, leading to very low voltage device operation at ±15 V, as shown in our previous work.[32] The low-voltage operation was even more difficult in top-gate FETs, in which only a few interlayers were available that do not cause damage to the organic semiconductor underneath. Nanocomposite of P(VDF-TrFE) and high-*k* ferroelectric nanoparticles such as $BaTiO_3$ can be a good way for this purpose and a preliminary study is under way.

Device switching properties are also of prime importance for real implementation.[38] Apparently the switching operation of a FET strongly depends on the field-effect mobility of semiconductor, but, in addition, in our hysteresis-free device, it relies upon the polarization switching speed of the P(VDF-TrFE) as well. The field-effect mobility of our device was approximately 0.5 cm^2 V^{-1} s^{-1}, comparable with conventional organic and polymeric ones, which implies that our device can be potentially useful for the applications that organic field-effect transistors are targeting. Although intrinsic switching of a P(VDF-TrFE) occurred at a level of approximately a few nanoseconds, its switching speed was varied, depending on the types of

devices.[29] For instance, metal/ferroelectric/metal capacitors showed, in general, a switching time on the order of microseconds, while field-effect-transistor-type devices exhibited a switching time of 10^{-3} to 10^{-4} seconds. The literature, therefore, suggests that our FET device can be useful for applications requiring a kHz-level frequency operation. A specific application in which our near-hysteresis-free networked SWNT FET can be useful is a near-IR photodetector, in which we are able to measure the characteristic source-drain current arising from photocarriers generated upon preferential near-IR absorption of SWNTs. This type of photosensor in general does not require a high switching rate, but a highly dispersed networked SWNT channel with multiple Schottky junctions[24] is essential not only for the production of plentiful photocarriers but also for their facilitated transportation to the electrode.

3. Conclusions

In this study, we have developed a simple and robust method that effectively controls the characteristic current hysteresis of SWNTs by non-volatile ferroelectric polarization. A ferroelectric P(VDF-TrFE) gate insulator employed as a top-gate FET with a solution-processed SWNT-network channel layer suppressed the current hysteresis when the gate-voltage sweep exceeded the coercive voltage of the P(VDF-TrFE) film. Near-hysteresis-free operation of the device was realized at a gate voltage above the onset voltage, which scales linearly down to a few volts with the thickness of the ferroelectric film by extrapolation. The various transient charges around the SWNTs responsible for the current hysteresis were compensated for by bistable, permanent polarizations that developed at gate-voltage sweeps greater than the coercive field voltage of the ferroelectric layer. This approach opens a new device-fabrication scheme for environmentally stable hysteresis-free SWNT-network FETs.

4. Experimental Section

Materials and Dispersion of SWNTs: Purified arc-discharge single-walled carbon nanotubes (SWNTs) produced at Hanwha Nanotech, Grade ASP-100F, were used as received. A poly(styrene-*block*-paraphenylene) (PS-*b*-PPP) copolymer polyphenylene-rich in 1,4-additions was synthesized by the dehydrogenation of poly(styrene-*block*-1,4-cyclohexadiene) from Polymer Source Inc., Doval, Canada. The molecular weights of the PS and PPP were 4800 g mol^{-1} and 1100 g mol^{-1}, respectively. The block copolymer was amorphous, and the glass-transition temperatures of the PS and PPP blocks were 83 and 177 °C, respectively. The polydispersity index (PDI) of the PS-*b*-PPP (5k/1k) was 1.10. P(VDF-TrFE) with 27.5 wt% TrFE was purchased from MSI Sensors. The melting (T_m) and Curie (T_c) temperatures of the P(VDF-TrFE) were 160 and 80 °C, respectively. All of the organic solvents, including methyl ethyl ketone (MEK) and THF, were purchased from Sigma–Aldrich Korea.

To investigate the electrical characteristics of the thin, networked SWNT films, various amounts of SWNTs were dispersed in a 1 mg mL^{-1} PS-*b*-PPP (5k/1k) (0.1 wt%) THF solution. The appropriate amount of a 0.5 mg mL^{-1} THF stock solution of SWNTs, prepared by brief sonication, was added to the polymer solution in THF, which allowed control of the concentration of the SWNTs dispersed in the polymer solution. The mixtures were horn-sonicated for 5 min (VC 750, Sonics & Materials, Inc.), followed by a ten-minute bath sonication. To increase the proportion of individually dispersed nanotubes, the sonicated solutions were further centrifuged at different rotor speeds ranging from 9500 to 16 500 rpm, and the upper parts were subsequently carefully decanted.

Device Fabrication: Metal/P(VDF-TrFE)/metal capacitors were made with thermally evaporated Au bottom and top electrodes. The Au top electrodes were thermally evaporated on the polymer films, spin coated on a flat Au bottom electrode surface using a shadow mask with holes of 200 μm in diameter under a pressure of 10^{-6} mbar and at rate of 0.1 nm s^{-1}. The ferroelectric properties were obtained using a virtual ground circuit (Radiant Technologies Precision LC unit). For the fabrication of the FETs with networked SWNTs, the bare, sonicated solutions and the decanted ones were spin-coated at 1000 rpm on 200 nm-thick SiO_2 insulators thermally grown on highly degenerate boron-doped silicon wafers to generate the gate electrodes. Some of the samples were thermally annealed at 190 °C for 24 h and 380 °C for 30 min. Device fabrication was completed by thermal evaporation of Au through shadow SUS-masks for the source and drain electrodes, which had channel lengths and widths of 100 μm and 2000 μm, respectively, resulting in 18 devices with a bottom-gate and top-contact configuration. To fabricate the top-gate FETs with the ferroelectric P(VDF-TrFE) gate insulators, various P(VDF-TrFE) solutions in MEK at different concentrations were directly spin-coated on the previously prepared bottom-gate top-contact FETs. Subsequent deposition of a Au gate electrode by thermal evaporation gave rise to top-gate bottom-contact FETs with different P(VDF-TrFE) film thicknesses, as illustrated in Figure 1a.

Characterization: The nanostructures of the SWNT/PS-*b*-PPP(5k/1k) composite films were observed by high-resolution TEM (HR-TEM) (JEOL 2100F) at 200 kV in the bright field. The electrical characteristics were measured by semiconductor systems (E5270B, Agilent Technologies). All of the measurements were done in a metallic dark box at room temperature in air. We employed a standard gate-voltage cycle rate that our apparatus supported, 16.61 ms per step. The step increase of the voltage corresponded to 0.1 V per step. All of the measurements we performed for device characterization were based on the DC mode.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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